EXAMINER'S SEARCH NOTES

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United States Patent [19]

Yuen

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[54] **MASTER SLICE GATE ARRAY INTEGRATED CIRCUITS WITH BASIC CELLS ADAPTABLE FOR BOTH INPUT/OUTPUT AND LOGIC FUNCTIONS**

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[73] Assignee: **Quality Semiconductor, Inc.**, Santa Clara, Calif.

[21] Appl. No.: **995,224**

[22] Filed: **Dec. 22, 1992**

[51] **Int. Cl.**[5] **H01L 27/02**

[52] **U.S. Cl.** **257/401**; 257/202; 257/206

[58] **Field of Search** 257/202, 203, 204, 206, 257/207, 208, 287, 338, 350, 358, 401, 390, 365

[56] **References Cited**

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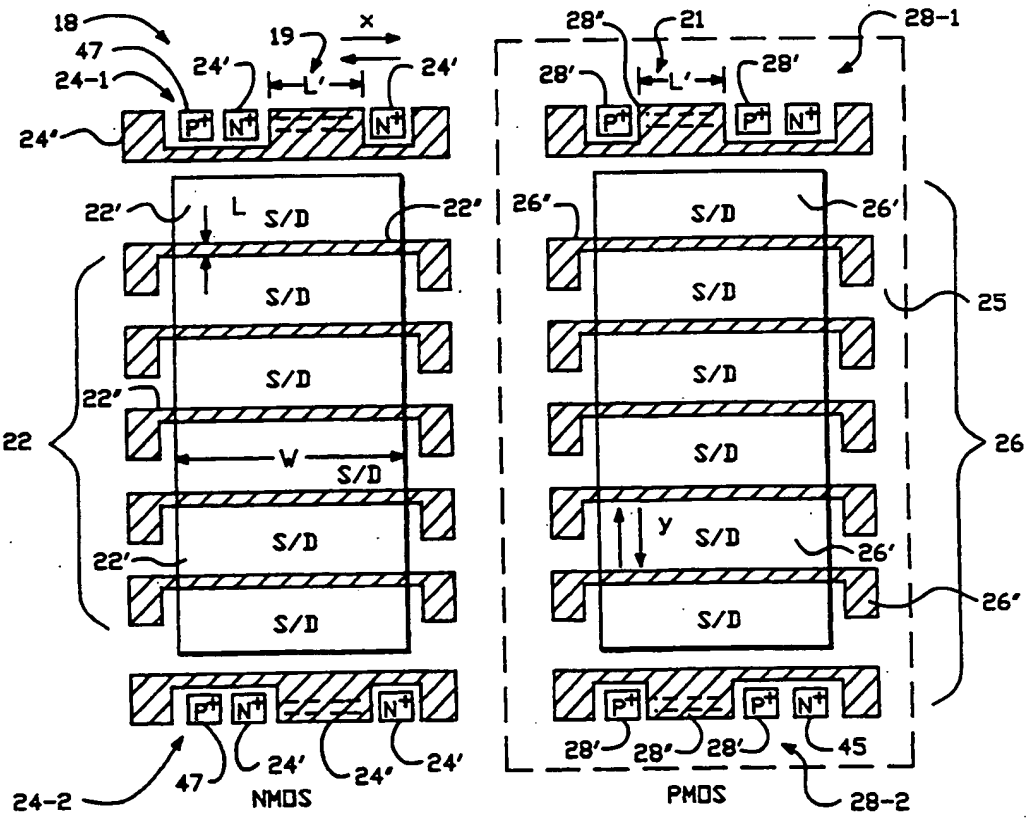
[57] **ABSTRACT**

The input/output circuit cells of a master-slice gate array device have the same diffusion and gate regions as the basic transistors so that the input/output of the device may be defined at the metallization stage rather than at the time the diffusion regions are formed. Thus a single size master-slice circuit device need to be kept in inventory. The array size is selected in accordance with the customer's specification and the inputs/outputs are defined accordingly using CAD. Thereafter, the die may be scribed into smaller. The transistors for sea-of-gate structures containing a pair of long channel transistors whose drain, gate and source regions lie on a single grid or track of the CAD design tool. By using a long channel transistor in the feedback loop of a memory cell, gating transistors may be eliminated to reduce transistors required for latches. To provide the required drive capability, a number of transistors may be connected to form the input or output buffer, without requiring large transistors with large diffusion regions. A metal silicide resistor and a number of discharge transistors normally in the off condition are connected to the node between an input/output pad and input/output buffer for electrostatic discharge.

23 Claims, 10 Drawing Sheets



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DOCUMENT-IDENTIFIER:	US 5367187 A
TITLE:	Master slice gate array integrated circuits with basic cells adaptable for both input/output and logic functions

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Abstract Text - ABTX (1):

The input/output circuit cells of a master-slice gate array device have the same diffusion and gate regions as the basic transistors so that the input/output of the device may be defined at the metallization stage rather than at the time the diffusion regions are formed. Thus a single size master-slice circuit device need to be kept in **inventory**. The array size is selected in accordance with the customer's specification and the inputs/outputs are defined accordingly using CAD. Thereafter, the die may be scribed into smaller. The transistors for sea-of-gate structures containing a pair of long channel transistors whose drain, gate and source regions lie on a single grid or track of the CAD design tool. By using a long channel transistor in the feedback loop of a memory cell, gating transistors may be eliminated to reduce transistors required for latches. To provide the required drive capability, a number of transistors may be connected to form the input or output buffer, without requiring large transistors with large diffusion regions. A metal silicide resistor and a number of discharge transistors normally in the off condition are connected to the node between an input/output pad and input/output buffer for electrostatic discharge.

Brief Summary Text - BSTX (3):

In the semiconductor industry, a number of different design approaches have been used in the design and manufacture of integrated circuits. Two such approaches are custom logic and semi-custom logic. **Custom** logic typically requires expensive **custom** design to provide a made-to-order **integrated circuit** for specific functions. Even though **custom integrated circuits** are costly to design, they may be cost effective for large quantity production.

Brief Summary Text - BSTX (4):

For devices which are to be produced in small or moderate quantities, semi-**custom integrated circuits** may be more cost effective. Semi-custom logic includes programmable array logic (PAL) where the "programming" is performed after the fabrication of the device has been completed, such as by blowing fuses using lasers. PAL type circuits, however, are typically limited in the number of gate counts that can be included. For integrated circuits requiring a large number of gates, master-slice gate array circuits are frequently used.